LMZ21700 650mA SIMPLE SWITCHER® Nano Module with 17V Maximum Input Voltage

Check for Samples: LMZ21700

FEATURES

- **Integrated Inductor**
- **Miniature 3.5 mm x 3.5 mm x 1.7 mm Package**
- **-40°C to 125°C Junction Temperature Range**
- **Adjustable Output Voltage**
- **Integrated Compensation**
- **Requires Only 10µF of Output Capacitance**
- **Adjustable Soft Start Function**
- **Starts into Pre-Biased Loads**
- **Power Good and Enable Pins**
- **Seamless Transition to Power-Save Mode**

APPLICATIONS

- **Point of Load Conversions from 5V and 12V**
- **Space Constrained Applications**
- **LDO Replacement**

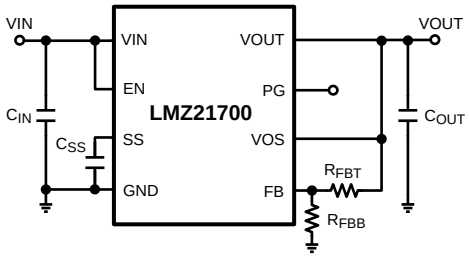
ELECTRICAL SPECIFICATIONS

- **Up to 650mA Output Current**
- **Input Voltage Range 3V to 17V**
- **Output Voltage Range 0.9V to 6V**
- **Efficiency up to 95%**
- **1.5µA Shutdown Current**
- **17µA Quiescent Current**

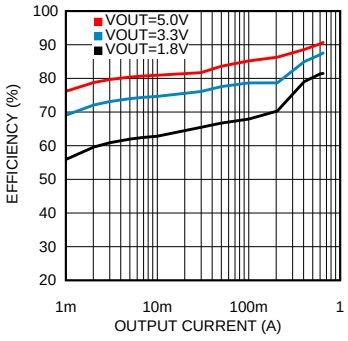
DESCRIPTION

The LMZ21700 SIMPLE SWITCHER Nano Module is an easy-to-use step-down DC-DC solution capable of driving up to 650mA load in space-constrained applications. Only an input capacitor, an output capacitor, a softstart capacitor, and two resistors are required for basic operation.

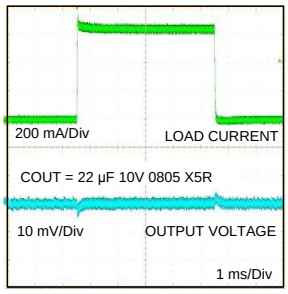
Typical Schematic



Typical Efficiency for V_{IN}=12V



Load Transient Response
0% to 100% Load Step



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Connection Diagram

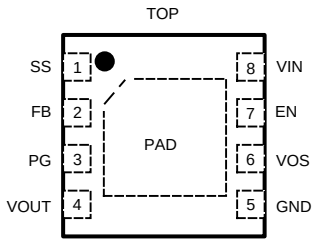

Figure 1.
DFN–8 pinout

PIN DESCRIPTIONS

Pin #	Name	Description
1	SS	Soft-start pin. An external capacitor connected to this pin sets the internal voltage reference ramp time. It can be used for tracking and sequencing.
2	FB	Voltage feedback. Connect resistive voltage divider to this pin to set the output voltage.

PIN DESCRIPTIONS (continued)

Pin #	Name	Description
3	PG	Output power good (High = VOUT ready, Low = VOUT below nominal regulation); open drain (requires pull-up resistor; goes high impedance, when device is switched off)
4	VOUT	Output Voltage. Connected to one terminal of the integrated inductor. Connect output filter capacitor between VOUT and PGND.
5	GND	Ground for the power MOSFETs and gate-drive circuitry.
6	VOS	Output voltage sense pin and connection for the control loop circuitry.
7	EN	Enable input (High = enabled, Low = disabled). Internal pull down resistor keeps logic level low if pin is left floating
8	VIN	Supply voltage for control circuitry and power stage.
	PAD	Electrically connected to GND. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

VIN	−0.3V to +20V
EN, SS	−0.3V to (VIN +0.3V) w/20V max
FB, PG, VOS	-0.3V to 7V
PG sink current	10mA max
Junction Temperature ($T_{J\text{-}MAX}$)	+150°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature	TBD
ESD Susceptibility	±2kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

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Operating Ratings(1)

Input Voltage Range	3V to 17V
Recommended Load Current	0 mA to 650 mA
Junction Temperature (T_J) Range	−40°C to +125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), SYB08A Package(1)	TBD°C/W

(1) Junction-to-ambient thermal resistance (θ_{JA}) is based on 4 layer board thermal measurements, performed under the conditions and guidelines set forth in the JEDEC standards JESD51-1 to JESD51-11. θ_{JA} varies with PCB copper area, power dissipation, and airflow.

Electrical Characteristics(1)

Specifications with standard typeface are for T_J = 25°C only; Limits in **bold face** type apply over the operating junction temperature range T_J of -40°C to 125°C. Minimum and maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12V.

Symbol	Parameter	Conditions	Min(1)	Typ(2)	Max(1)	Units
SYSTEM PARAMETERS						
I_Q	Operating quiescent current	EN = high, I_{OUT}=0mA, device not switching		17	**25**	µA
I_{SD}	Shutdown current	EN = low		1.5	**4**	µA
VIN_{UVLO}	Input under voltage lock out rising threshold		**2.8**	2.9	**3**	V
$VIN_{UVLO-HYS}$	Input under voltage lock out hysteresis				**0.2**	V
T_{SD}	Thermal shutdown	Rising Threshold		160		°C
$T_{SD-HYST}$	Thermal shutdown hysteresis			20		°C
CONTROL						
$V_{IH, ENABLE}$	Enable logic HIGH voltage		**0.9**			V
$V_{IL, ENABLE}$	Enable logic LOW voltage				**0.3**	V
I_{LKG}	Input leakage current	EN=VIN or GND		0.01	**1**	µA
V_{TH_PG}	Power Good threshold voltage	Rising (%VOUT)	**92**	95	**98**	%
		Falling (%VOUT)	**87**	90	**93**	%
V_{OL_PG}	Power Good output low voltage	I_{PG}= -2mA		0.07	**0.3**	V
I_{LKG_PG}	Power Good leakage current	V_{PG}=1.8V		1	**400**	nA
I_{SS}	Softstart pin source current		**2.3**	2.5	**2.7**	µA
POWER STAGE						
$R_{DS(ON)}$	High-Side MOSFET ON Resistance	V_{IN}≥6V		90		mΩ
		V_{IN}=3V		120		
	Low-Side MOSFET ON Resistance	V_{IN}≥6V		40		mΩ
		V_{IN}=3V		50		
L	Integrated power inductor value			2.2		µH
DCR	Integrated power inductor DC resistance			100		mΩ
I_{CL}	Output (DC) current limit	TBD	**0.8**	0.9		A
OUTPUT						
V_{REF}	Internal reference voltage			0.8		V

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.

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Electrical Characteristics[1] (continued)

Specifications with standard typeface are for T_J = 25°C only; Limits in **bold face** type apply over the operating junction temperature range T_J of -40°C to 125°C. Minimum and maximum limits are guaranteed through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12V.

Symbol	Parameter	Conditions	Min[1]	Typ[2]	Max[1]	Units
SYSTEM PARAMETERS						
I_{FB}	Feedback pin leakage current	V_{FB}=0.8V		1	**100**	nA
V_{OUT}	Initial output voltage accuracy	PWM Mode $V_{IN} \geq V_{OUT + 1V}$	**-1.8**		**1.8**	%
		Power save mode C_{OUT}=22µF	**-2.3**		**2.8**	%
	Load regulation	V_{IN}=12V, V_{OUT}=3.3V, PWM mode operation		0.05		%/A
	Line regulation	3V ≤ V_{IN} ≤ 17V, V_{OUT}= 3.3V, I_{OUT} = 650mA, PWM mode operation		0.02		%/V
THERMAL PERFORMANCE						
θ_{JA}	Package junction to ambient thermal resistance on PCB with 2 layers 35µm copper thickness 5 thermal vias under package	10x10mm copper area		TBD		°C/W
		15x15mm copper area		TBD		
		20x20mm copper area		TBD		

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System Characteristics

The following specifications are guaranteed by design providing the component values in the Typical Application Circuit are used (C_{IN} = C_{OUT} = 10 µF). **These parameters are not guaranteed by production testing.** Unless otherwise stated the following conditions apply: T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$\Delta V_{OUT}/V_{OUT}$	Output Voltage Regulation Over Line Voltage and Load Current	V_{OUT} = 1.2V ΔV_{IN} =3V to 17V ΔI_{OUT} = 0A to 0.65A		±TBD		%
$\Delta V_{OUT}/V_{OUT}$	Output Voltage Regulation Over Line Voltage and Load Current	V_{OUT} = 1.8V ΔV_{IN} =3V to 17V ΔI_{OUT} = 0A to 0.65A		±TBD		%
$\Delta V_{OUT}/V_{OUT}$	Output Voltage Regulation Over Line Voltage and Load Current	V_{OUT} =2.5V ΔV_{IN} =3V to 17V ΔI_{OUT} = 0A to 0.65A		±TBD		%
$\Delta V_{OUT}/V_{OUT}$	Output Voltage Regulation Over Line Voltage and Load Current	V_{OUT} =3.3V ΔV_{IN} =5V to 17V ΔI_{OUT} = 0A to 0.65A		±TBD		%
$\Delta V_{OUT}/V_{OUT}$	Output Voltage Regulation Over Line Voltage and Load Current	V_{OUT} =5V ΔV_{IN} =7V to 17V ΔI_{OUT} = 0A to 0.65A		±TBD		%
η	Peak Efficiency	V_{IN} = 12V, V_{OUT} = 3.3V I_{OUT} = 650 mA		87.6		%
	Light Load Efficiency	V_{IN} = 12V, V_{OUT} = 3.3V I_{OUT} = 1 mA		70		
V_{OUT} Ripple	Output voltage ripple	V_{IN} =12V, V_{OUT} = 3.3V I_{OUT} = 650mA		tbd		mV pk-pk
Line Transient	Line transient response	TBD		tbd		mV pk-pk
Load Transient	Load transient response	TBD		tbd		mV pk-pk

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Typical Performance Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 12V, T_A = 25°C

Graph 1

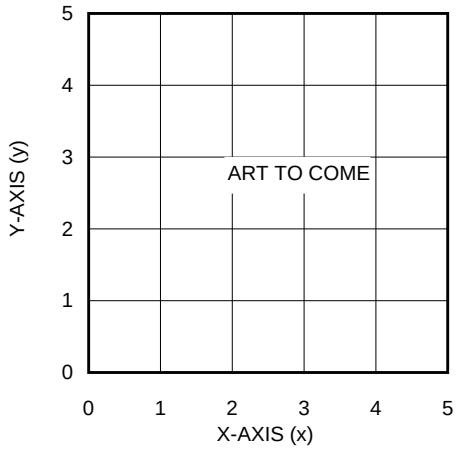

Figure 2.

Graph 2

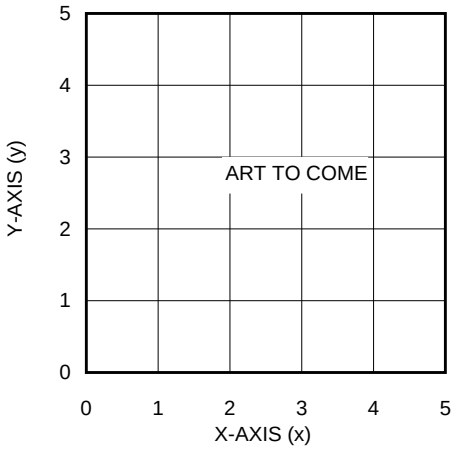

Figure 3.

Graph 3

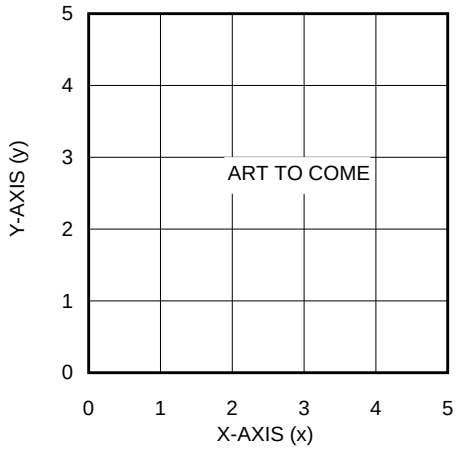

Figure 4.

Graph 4

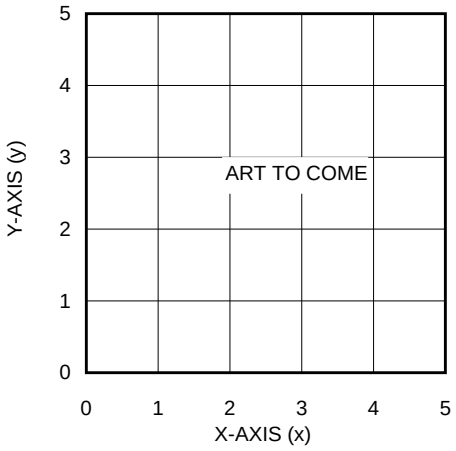

Figure 5.

Graph 5

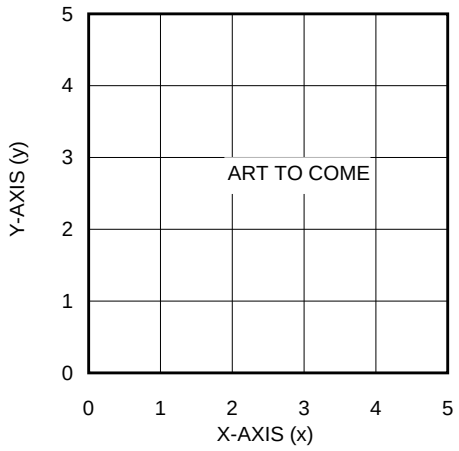

Figure 6.

Graph 6

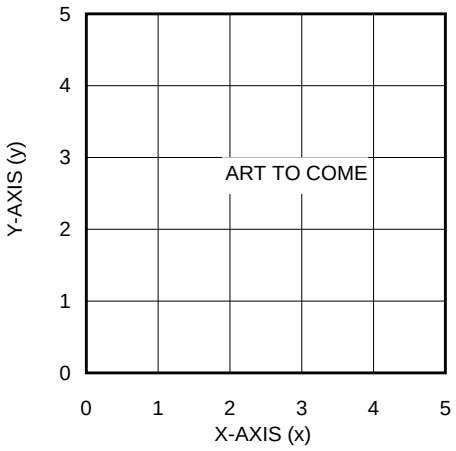

Figure 7.

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APPLICATIONS INFORMATION

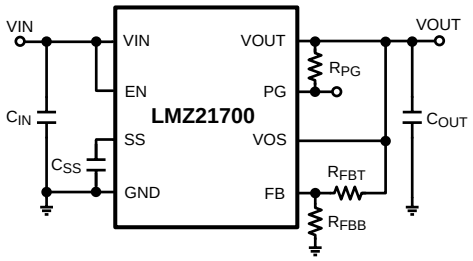

Figure 8. Typical Applications Circuit

Overview

The LMZ21700 SIMPLE SWITCHER Nano Module is an easy-to-use step-down DC-DC solution capable of driving up to 650mA load in space-constrained applications. Only an input capacitor, an output capacitor, a softstart capacitor, and two resistors are required for basic operation. The nano module comes in 8-pin DFN footprint package with an integrated inductor. The LMZ21700 architecture is based on DCS-Control (Direct Control with Seamless Transition into Power Save Mode). This architecture combines the fast transient response and stability of hysteretic type converters along with the accurate DC output regulation of voltage mode and current mode regulators.

The LMZ21700 architecture uses Pulse Width Modulation (PWM) mode for medium and heavy load requirements and Power Save Mode (PSM) at light loads for high efficiency. In PWM mode the switching frequency is controlled over the input voltage range. The value depends on the output voltage setting and is typically reduced at low output voltages to achieve higher efficiency. In PSM mode the switching frequency decreases linearly with the load current. Since the architecture of the device supports both operation modes (PWM and PSM) in a single circuit building block, the transition between the modes of operation is seamless with minimal effect on the output voltage.

PWM Mode Operation

The LMZ21700 operates in PWM mode when the output current is greater than half the inductor ripple current. The operating frequency is nominally set for 2.5MHz. The frequency variation in PWM mode is controlled and depends on the V_{IN} and V_{OUT} settings. Refer to the Typical Performance Characteristics section for switching frequency graphs for several typical output voltage settings. As the load current is decreased and the valley of the inductor current ripple reaches 0A the device enters PSM mode of operation to maintain high efficiency.

PSM Mode Operation

Once the load current decreases the LMZ21700 will transition to Power Save Mode of operation. The device will remain in PSM mode as long as the inductor current is discontinuous. The switching frequency will decrease linearly with the load current. If V_{IN} decreases to about 15% above V_{OUT} the device will not enter PSM mode and will maintain output regulation in PWM mode.

Input Under Voltage Lockout

The LMZ21700 features input voltage lockout (UVLO) circuit. It monitors the input voltage level and prevents the device from switching the power MOSFETs if V_{IN} is not high enough. The typical V_{IN} UVLO rising threshold is 2.9V with 200mV of hysteresis.

Enable Input (EN)

The Enable pin (EN) pin is weakly pulled down internally through a 400kΩ resistor to keep EN logic low when the pin is floating. The pull-down resistor is not connected when EN is set high. Once the voltage on the Enable pin (EN) is set High the nano module will start operation. If EN is set Low the LMZ21700 will enter shutdown mode. The typical shutdown quiescent current is 1.5µA.

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Softstart and Tracking Function (SS)

When EN is set high for device operation the LMZ21700 will start switching after 50µs delay and the output voltage will start rising. The V_{OUT} rising slope is controlled by the external capacitor Css connected to the Softstart (SS) pin. The nano module has a 2.5µA constant current source internally connected to the SS pin to program the softstart time Tss:

$T_{SS} = C_{SS}$ x 1.25V / 2.5µA

The softstart capacitor voltage is reset to zero when EN is pulled low and when the thermal protection is active.

If tracking function is desired, the SS pin can be used to track external voltage. If the applied external tracking voltage is between 50mV and 1.2V, the FB voltage will follow SS according to the following relationship:

$V_{FB} = 0.64$ x V_{SS}

Power Good Function (PG)

The LMZ21700 features a power good function which can be used for sequencing of multiple rails. The PG pin is an open-drain output and requires a pull-up resistor R_{PG} to V_{OUT} (or any other external voltage less than 7V). When the nano module is enabled and UVLO is satisfied, the power good function starts monitoring the output voltage. The PG pin is kept at logic low if the output has not reached the proper regulation voltage. Refer to the Electrical Characteristics table for the PG voltage thresholds. The PG pin can sink 2mA of current which sets the minimum limit of the R_{PG} resistance value:

$R_{PG\text{-}MIN} = V_{PULL\text{-}UP}$ / 2mA

The PG pin goes high impedance if the device is disabled or the thermal protection is active.

Output Voltage Setting

The output voltage of the LMZ21700 is set by a resistive divider from V_{OUT} to GND, connected to the feedback (FB) pin. The output voltage can be set between 0.9V and 6V. The voltage at the FB pin is regulated to 0.8V. The recommended minimum divider current is 2µA. This sets a maximum limit on the bottom feedback resistor R_{FBB}. Its value should not exceed 400kΩ. The top feedback resistor R_{FBT} can be calculated using the following formula:

$R_{FBT} = R_{FBB}$ x (V_{OUT}/ 0.8 – 1)

Output Current Limit and Output Short Circuit Protection

The LMZ21700 has integrated protection against heavy loads and output short circuit events. Both, the high-side FET and low-side FET have current monitoring circuitry. If the current limit threshold of the high-side FET is reached , the high-side FET will be turned off and the low-side FET will be turned on to sink the inductor current. Once the current through the low-side FET has decreased below a safe level, the high-side device will be allowed to turn on again. The actual DC output current depends on the input voltage, output voltage, and switching frequency. Refer to the Typical Performance Curves for more information.

Thermal Protection

The nano module monitors its junction temperature (Tj) and shuts itself off if the it gets too hot. The thermal shutdown threshold for the junction is 160°C. Both, high-side and low-side FETs are turned off until the junction temperature has decreased under the hysteresis level, typically 20°C below the shutdown temperature.

External Components Selection

Input Capacitor (C_{IN})

The LMZ21700 is designed for use with low ESR multi-layer ceramic capacitors (MLCC) for its input filter. Using a 10 µF 0805 or larger with 25V or larger rating ceramic input capacitor typically provides sufficient VIN bypass. Use of multiple 4.7 µF capacitors can also be considered. Ceramic capacitors with X5R and X7R temperature characteristics are recommended for C_{IN}. These provide an optimal balance between small size, cost, reliability, and performance for space sensitive applications. The DC voltage bias characteristics of the capacitors must be considered when selecting the DC voltage rating and case size of these components. The effective capacitance of an MLCC is typically reduced by the DC voltage bias applied across its terminals.

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Output Capacitor (C_{OUT})

Similarly to the input capacitor, it is recommended to use low ESR multi-layer ceramic capacitors for C_{OUT}. Ceramic capacitors with X5R and X7R temperature characteristics are recommended. Use 10 µF or larger value and consider the DC voltage bias characteristics of the capacitor when choosing the case size and voltage rating. For stability, the output capacitor should be in the 10 µF – 200 µF range.

Softstart Capacitor (C_{SS})

The softstart capacitor is chosen according to the desired softstart time. As described in the Softstart and Tracking Function section the softstart time $T_{SS} = C_{SS}$ x 1.25V / 2.5µA.

A minimum C_{SS} value of 1000pF is required for monotonic V_{OUT} ramp up.

Power Good Resistor (R_{PG})

If the Power Good function is used, a pull up resistor R_{PG} is necessary from the PG pin to an external pull-up voltage.

The minimum R_{PG} value is restricted by the pull down current capability.

$R_{PG-MIN} = V_{PULL-UP} / 2mA$

The maximum R_{PG} value is based on the maximum PG leakage current and the minimum “logic high” level system requirements:

$R_{PG-MAX} = (V_{PULL-UP} – V_{LOGIC-HIGH}) / I_{LKG\_PG}$

Feedback Resistors (R_{FBB} and R_{FBT})

The feedback resistors R_{FBB} and R_{FBT} set the desired output voltage. Choose R_{FBB} value less than 400kΩ and calculate the value for R_{FBT} using the following formula:

$R_{FBT} = R_{FBB}$ x $(V_{OUT} / 0.8 – 1)$

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REVISION HISTORY

Changes from Revision splat (August 2012) to Revision A	Page
• Changed Description	1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMZ21700SILR	PREVIEW	uSiP	SIL	8	3000	TBD	Call TI	Call TI	-40 to 125		
LMZ21700SILT	PREVIEW	uSiP	SIL	8	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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